XILINX

XQ Versal™ ACAP Portfolio Product Selection Guide

Industry's First Adaptive Compute Acceleration Platform (ACAP)

XQ Ruggedized Versal™ AI Core Series – Resources

		VC1352	VC1702	VC1902
Intelligent Engines	AI Engines Tiles	128	304	400
	AI Engine-ML Tiles	0	0	0
	AI Engine Data Memory (Mb)	32	76	100
	AIE-ML Shared Memory (Mb)	0	0	0
	DSP Engines	928	1,312	1,968
Adaptable Engines	System Logic Cells (K)	540	981	1,968
	LUTs	246,784	448,512	899,840
	NoC Master / NoC Slave Ports	10	21	28
	Distributed RAM (Mb)	8	14	27
Memory	Total Block RAM (Mb)	16	34	34
	UltraRAM (Mb)	59	130	130
	Accelerator RAM (Mb)	32	0	0
	Total PL Memory (Mb)	115	178	191
	DDR Memory Controllers	2	3	4
	DDR Bus Width	128	192	256
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC		
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC		
	Memory	256KB On-Chip Memory w/ECC		
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)		
Serial Transceivers	GTY Transceivers (32.75Gb/s)	0	44	44
	GTYP Transceivers (32.75Gb/s)	8	0	0
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	–	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX
	PCI Express®	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	100G Multirate Ethernet MAC	1	4	4
	Platform Management Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug		
Speed, Voltage, Power, and Temperature	Military Temp	1MSM		
	Industrial Temp	1LSI, 1MSI, 2MSI		

All parameters listed are maximum values in XC product variant.

XQ Ruggedized Versal™ AI Core Series – Packaging

			VC1352	VC1702	VC1902
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP		
NBRA1024	31x31	0.92	168, 210 22, 78 0, 8		
NSRE1369	35x35	0.92	168, 210, 44, 78 0, 8		
NSRG1369	35x35	0.92		132, 246 44, 78 0, 24	
VSRA1596(1)	37.5x37.5	0.92		132, 246 44, 78 0, 32	
VIRA1596(1)	40x40	0.92			132, 246 44, 78 32, 0
VSRD1760	40x40	0.92			186, 462 0, 78 24, 0
VSRA2197	45x45	0.92		192, 294 44, 78 0, 44	186, 462 44, 78 44, 0

Notes:
1. LPDDR4 is supported in 324 I/O only.

All parameters listed are maximum values in XC product variant.

XQ Ruggedized Versal™ AI Edge Series – Resources

		VE2102	VE2302
Intelligent Engines	AI Engine-ML Tiles	12	34
	AI Engine Tiles	0	0
	AIE/AIE-ML Data Memory (Mb)	6	17
	AIE-ML Shared Memory (Mb)	48	68
	DSP Engines	176	464
Adaptable Engines	System Logic Cells	80,080	328,720
	LUTs	36,608	150,272
	NoC Master / NoC Slave Ports	2	5
	Distributed RAM (Mb)	1.1	4.6
Memory	Total Block RAM (Mb)	1.7	5.4
	UltraRAM (Mb)	13.2	43.6
	Accelerator RAM (Mb)	32	32
	Total PL Memory (Mb)	48	85.6
	DDR Memory Controllers	1	1
	DDR Bus Width	64	64
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC	
	Real-Time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC	
	Memory	256KB On-Chip Memory w/ECC	
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)	
Serial Transceivers	GTY Transceivers (32.75Gb/s)	0	0
	GTYP Transceivers (32.75Gb/s)	0	8
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	-	-
	PCI Express®	-	1 x Gen4x8
	40G Multirate Ethernet MAC	0	1
	Platform Mgmt Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug	
Speed, Voltage, Power, and Temperature	Military Temp	1MSM	
	Industrial Temp	1LSI, 1MSI, 2MSI	

All parameters listed are maximum values in XC product variant.

XQ Ruggedized Versal™ AI Edge Series – Packages

			VE2102	VE2302
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP	
SBRA484	19x19	0.8	84, 30 0, 78 0, 0	
SSRA784	23x23	0.8	132, 84 0, 78 0, 0	132, 84 22, 78 0, 8

All parameters listed are maximum values in XC product variant.

XQ Ruggedized Versal™ Prime Series – Resources

		VM1102	VM1402	VM1502	VM1802
Adaptable Engines	System Logic Cells (K)	329	1,238	981	1,968
	LUTs	150,272	565,760	448,512	899,840
	NoC Master / NoC Slave Ports	5	18	21	28
	Distributed RAM (Mb)	5	17	14	27
Memory	Total Block RAM (Mb)	5	40	34	34
	Total UltraRAM (Mb)	44	80	130	130
	Total PL Memory (Mb)	54	137	178	191
	DDR Memory Controllers	1	4	3	4
	DDR Bus Widths	64	256	192	256
Intelligent Engines	DSP Engines	464	1,696	1,312	1,968
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC			
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC			
	Memory	256KB On-Chip Memory w/ECC			
	Connectivity	Ethernet (x2); USB 2.0 (x1); UART (x2); SPI (x2); I2C (x2); CAN-FD (x2)			
Serial Transceivers	GTY Transceivers (32.75Gb/s)	0	24	44	44
	GTYP Transceivers (32.75Gb/s)	8	0	0	0
	GTM Transceivers (56Gb/s)	0	0	0	0
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX
	PCI Express®	1 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	100G Multirate Ethernet MAC	1	2	4	4
Speed, Voltage, Power, and Temperature	Military Temp	1MSM			
	Industrial Temp	1LSI, 1MSI, 2MSI			

Notes:
1. 16 GTYP transceivers are dedicated to the CPM for PCI Express use.

All parameters listed are maximum values in XC product variant.

XQ Ruggedized Versal™ Prime Series – Packaging

			VM1102	VM1402	VM1502	VM1802
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP, GTM			
SSRA784	23x23	0.8	132, 84 22, 78 0, 8, 0			
NSRB1369	35x35	0.92		132, 192 22, 78 24, 0, 0		
VSRC1596	37.5x37.5	0.92		168, 480 22, 78 24, 0, 0		
VSRD1760(2)	40x40	0.92		168, 480 0, 78 16, 0, 0		186, 462 0, 78 24, 0, 0
VSRA2197	45x45	0.92			192, 294 44, 78 44, 0, 0	186, 462 44, 78 44, 0, 0

Notes:
1. Some packages are compatible with Versal Premium series devices.
2. VM1402 in VSRD1760 supports LPDDR4 in 324 I/O only.

All parameters listed are maximum values in XC product variant.

XQ Ruggedized Versal™ Premium Series – Resources

		VP1202	VP1402	VP1502	VP1702
Adaptable Engines	System Logic Cells (K)	1,969	2,233	3,763	5,558
	LUTs	900,224	1,020,928	1,720,448	2,540,672
	NoC Master / NoC Slave Ports	28	42	52	76
	Distributed RAM (Mb)	27	31	53	78
Memory	Total Block RAM (Mb)	47	70	89	132
	UltraRAM (Mb)	190	181	366	541
	Total PL Memory (Mb)	264	282	508	751
	DDR Memory Controllers	4	3	4	4
	DDR Bus Width	256	192	256	256
Intelligent Engines	DSP Engines	3,984	2,672	7,440	10,896
Scalar Engines	APU	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC			
	RPU	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC			
	Memory	256KB On-Chip Memory w/ECC			
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)			
Serial Transceivers	GTYP Transceivers (32.75Gb/s)	28(1)	8	28(1)	28(1)
	GTM Transceivers(2) (58G (112G))	20 (10)	96 (48)	60 (30)	100 (50)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM5)	2 x Gen5x8, CCIX	-	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express®	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	2	6	4	6
	600G Ethernet MAC	1	8	3	5
	600G Interlaken	0	2	1	2
	400G High-Speed Crypto Engines	1	5	2	3
Speed, Voltage, Power, and Temperature	Military Temp	1MSM	1MSM	-	-
	Industrial Temp	1LSI, 1MSI, 2MSI			

Notes:
1. 16 GTYP transceivers are dedicated to the CPM5 for PCI Express use.
2. GTM transceivers can operate at data rates up to 112Gb/s by combining two transceivers together.

All parameters listed are maximum values in XC product variant.

XMP489 (v1.0)

XQ Ruggedized Versal™ Premium Series – Packaging

			VP1202	VP1402	VP1502	VP1702
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTYP, GTM (112G)			
VSRF1760(1)	40x40	0.92		180, 306 22, 78 8, 40 (20)		
VSRC2197(1)	45x45	0.92	132, 516 0, 78 28, 20 (10)			
VSRA2785(2)	50x50	0.92	132, 570 0, 78 28, 20 (10)	180, 306 44, 78 8, 80 (40)	132, 570 0, 78 28, 56 (28)	
VSRA3340	55x55	0.92			132, 354 0, 78 28, 60 (30)	132, 354 0, 78 28, 88 (44)

Notes:
1. Some packages are footprint compatible with Versal Prime series devices.
2. VP1202, and VP1502 in VSRA2785 support LPDDR4 in 486 I/O only.

XQ Ruggedized Versal™ ACAP Migration Table

Package XC / XQ	Footprint	Versal AI Edge Series							Versal AI Core Series							Versal Prime Series										Versal Premium Series						
		VE2002	VE2102	VE2202	VE2302	VE2602	VE1752	VE2802	VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802	VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902	VP1102	VP1202	VP1402	VP1502	VP1552	VP1702	VP1802
SBV / SBR	A484	●	■																													
SBV / –	A625	●	●																													
SFV / SSR	A784	●	■	●	■											■																
NBV / NBR	A1024								■																							
NBV / –	B1024																●	●														
NFV / NSR	B1369																●	■	●													
NSV / –	E1369								■																							
NSV / NSR	F1369																●	●														
NSV / NSR	G1369						●			●	■																					
NSV / –	H1369					●		●						●	●																	
VSV / VSR (1)	A1596						●			●	■																					
VIV / VIR (1)	A1596											■	●																			
VFV / VSR	C1596																●	■														
VFV / –	C1760																		●	●												
VSV / VSR	D1760											■	■				●	■	●	■												
VFV / VSR	F1760																				●	●			●	●	■					
VFV / –	H1760					●		●						●	●																	
VSV / VSR	A2197						●			●	■	●	■						●	■												
VSV / VSR	C2197																				●	●	■									
VSV / VSR	A2785																								●	■	■	■	●			
VSV / VSR	A3340																										●	■	●	■		
LSV / –	C4072																													●		

Legend
- ● No XQ Ruggedized Device
- ■ XQ Ruggedized Device
- **Migration Path**

Note:
1. Within the A1596 footprint packages: VSVA1596 and VSRA1596 package dimensions are 37.5x37.5mm, VIVA1596 and VIRA1596 package dimensions are 40x40mm with 1.25mm overhang

XQ Versal™ ACAP Ordering Information

Device Name				Device Attributes				Package Definition			
XQ	V	C	1902	-1	M	S	M	V	S	R	D1760
Xilinx XQ: Defense XC: Commercial XA: Automotive	**Architecture** Versal	**Series Name** E: AI Edge C: AI Core M: Prime P: Premium H: HBM	**Device Number** Digits 1-3: Value Identifier Digit 4: # of Primary Cores	**Speed Grade** -1: Slowest -2: Mid -3: Highest	**Voltage** L: Low (0.7V) M: Mid (0.80V) H: High (0.88V)	**Static Screen** S: Standard L: Low Static	**Temp Grade** M: –55 to +125°C I: –40 to 110°C(1)	**Ball Pitch** V: 0.92mm, w/LSC N: 0.92mm, no LSC S: 0.8mm L: 1.0mm	**Lid** S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring H: Lidded Overhang I: Lidless, w/Stiffener Ring & Overhang	**RoHS6 Code** R: Ruggedized, w/ eutectic Sn/Pb BGA Q: Non-ruggedized Sn/Pb BGA (2) V: Pb-free (in XC only)	**Footprint**

Note:
1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.
2. Non-ruggedized XQ version is available (the Sn/Pb BGA is added to any valid XC Versal ACAP I-temp product); consult your local Xilinx sales representative for further details.