PRODUCT BRIEF

Zynq™ UltraScale+™ MPSoC

OVERVIEW

Zynq™ UltraScale+™ MPSoCs combine a high-performance Arm®-based multicore, multiprocessing system (PS) with ASIC-class programmable logic (PL). These devices, equipped with dual- and quad-core application processors, deliver maximum scalability and are capable of offloading critical applications, such as graphics and video pipelining, to dedicated processing blocks. Zynq UltraScale+ MPSoCs also feature a full complement of integrated peripherals and connectivity cores suitable for next-generation systems.

Fully integrated programmable logic enables custom co-processors and custom memory hierarchies to meet application-specific needs, including deep learning processing units (DPU) for AI/ML processing. The 16nm FinFET+ programmable logic communicates with the processing system through 6,000 interconnects, enabling bandwidth that is not possible with multichip solutions. Dramatic power savings are achieved through fine-grained control of power domains and gated power islands. With specialized processing elements for different workloads, Zynq UltraScale+ MPSoCs are optimal single-chip platforms for both cost-sensitive and high-performance applications.

HIGHLIGHTS

Massive PS-PL Bandwidth Enables Efficient Accelerators

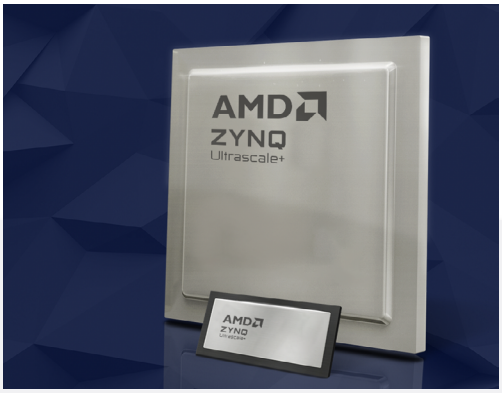
- 6,000 interconnects between PS and PL to avoid multi-chip I/O limitations
- Extensive library of hardened and soft peripheral IP enables many interfaces
- High-level language converts software bottlenecks into hardware accelerators
- Multi-port hardened controller enables PS and PL access to common memory

Packaging Innovation for Industry's Highest Compute Density

- Integrated Fan-Out (InFO) packaging for ultra-compact form factor (9.5x15mm)
- 60% less area (than flip-chip packaging) for better thermal & power distribution
- 5X compute density vs. comparable ASSPs (DMIPS/mm^2)
- Available for ZU1, ZU2, and ZU3 devices

Architectural Advantages vs. ASSPs

- Custom memory hierarchy for highest throughput, lowest latency designs
- Tightly coupled memory enables full isolation of safety-critical functions
- Soft co-processors for offloading or extra processing capability
- AI/ML processing capable with custom deep learning processing units (DPU)
- Scalable with the full Zynq MPSoC portfolio, preserving your design investment



TARGET APPLICATIONS

Industrial

- Machine Vision
- Industrial Networking (Time-Sensitive Networking)
- Industrial Controllers
- Retail Analytics
- Robotics
- Drives

Medical

- Portable and Desktop Ultrasound
- External Defibrillators
- Endoscopy

Automotive

- Monitoring Systems
- Camera-enabled Driver Assist Systems

AV Broadcasting

- Portable Pico Projectors
- Small Form Factor Broadcast

Aerospace & Defense

- MILCOM Radio
- Missiles & Munitions

FEATURES

	CG Devices	EG Devices	EV Devices
PROCESSING SYSTEM			
Application Processing Unit	Dual-core Arm® Cortex®-A53	Quad-core Arm Cortex-A53	Quad-core Arm Cortex-A53
Real-Time Processing Unit	Dual-core Arm Cortex-R5F	Dual-core Arm Cortex-R5F	Dual-core Arm Cortex-R5F
Graphics Processing Unit	–	Arm Mali™-400 MP2	Arm Mali-400 MP2
Video Codec Unit	–	–	Up to 8K @ 15fps Supports H.264/H.265
Embedded and External Memory	**Embedded:** 256KB On-Chip Memory w/ECC; 32KB L1 I/D Caches; 1MB L2 Cache **External:** DDR4/3/3L & LPDDR4/3 w/ECC; Quad-SPI; NAND w/ECC; eMMC		
PROGRAMMABLE LOGIC*			
System Logic Cells (K)	600	1,143	504
DSP Slices	2,520	3,528	1,728
Transceivers	24 @ 16Gb/s	44 @ 16Gb/s 28 @ 32Gb/s	24 @ 16Gb/s
On-Chip Memory (Mb)	44.2	80.4	44.2
PCIe® Gen3	2	5	2
Clock Management Tiles (CMTs)	8	11	8
High-Speed Connectivity	PCIe Gen2 x4; 2x USB3.0; SATA 3.1; DisplayPort; 4x Tri-mode Gigabit Ethernet		
FEATURES OVERVIEW			
Dynamic Power Management	> Multiple power domains with granular gating control > Platform Management Unit for power, safety, and reliability		
Safety and Security Features	> Configuration Security Unit for anti-tamper and lockdown > Support for 4096-bit RSA keys with SHA-3 hash functions > Secure system boot with AES 256 decryption > Full Arm TrustZone support		
Custom Memory Hierarchy	> Up to 10MB of internal local memory for co-processors and custom accelerators > Built-in DDR controller for low latency memory access > Tightly coupled memory enables isolated design flows for safety-critical applications		
Deep Learning Processing Unit (DPU) Compatible	> Configurable computation engine dedicated to convolutional neural networks > Accelerate AI/ML functions easily with reference designs and pre-built AI models		

*Maximum for each device family

TAKE THE NEXT STEP

Zynq UltraScale+ MPSoCs are supported by comprehensive development tools, reference designs, an IP catalog, and evaluation platforms. For more information about Zynq UltraScale+ MPSoCs, visit xilinx.com/zynq-ultrascale-plus. Evaluation kits sold separately; see the Zynq UltraScale+ MPSoC Kit Selection Guide for details and place an order today.

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